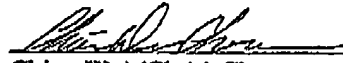


Attachment A

No.	Serial No	TSMC No.	Application Title	Filing Date	Assignment (Reel/Frame)
1	10/657,503	2002-0544	Phase Shift Assignments for Alternate PSM	9/8/03	014479/0625
2	10/425,322	2002-0382	Quartz Damage Repair Method for High-End Mask	4/29/03	014025/0791
3	10/661,746	2002-0353	Method to Shrink Cell Size in a Split Gate Flash	9/12/03	014500/0769
4	10/796,891	2002-0254B	Storage Element and SRAM Cell Structures Using Vertical FETS Controlled by Adjacent Junction Bias Through Shallow Trench Isolation	3/9/04	Recorded 014006/0344 at the parent application USP6,759,699
5	10/689,431	2002-0218	Method for Measuring Capacitance-Voltage Curves for Transistors	10/20/03	014622/0410
6	10/714,998	2002-0212	Water Soluble Negative Tone Photoresist	11/17/03	014712/0284
7	10/796,430	2002-0189	Placement and Routing Method to Reduce Joule Heating	3/9/04	015069/0548
8	10/307,646	2002-0132	Scheme for Eliminating the Channel Unexpected Turn-On During ESD Zapping	12/2/02	013547/0654
9	10/388,274	2002-0127	Light Guide for Image Sensor	3/12/03	013876/0368
10	10/256,401	2002-0064	Complementary Replacement of Material	9/27/02	013351/0995
11	10/788,175	2002-0047	Method for Making Improved Bottom Electrodes for Metal-Insulator-Metal Crown Capacitors	2/26/04	015033/0280
12	10/723,237	2001-1630	Method to Form a Robust TiCl ₄ Based CVD TiN Film	11/26/03	
13	10/755,500	2001-1596	Single Trench Repair Method with Etched Quartz for Attenuated Phase Shifting Mask	1/12/04	014896/0968
14	10/205,790	2001-1582	Full Sized Scattering Bar Alt-PSM Technique for IC Manufacturing in Sub-Resolution ERA	7/26/02	013148/0435

15	10/781,182	2001-1582D	Full Sized Scattering Bar Alt-PSM Technique for IC Manufacturing in Sub-Resolution ERA	2/18/04	Recorded 013148/0435 at the parent application USP6,711,732
16	10/781,176	2001-1582B	Full Sized Scattering Bar Alt-PSM Technique for IC Manufacturing in Sub-Resolution ERA	2/18/04	Recorded 013148/0435 at the parent application USP6,711,732
17	10/782,670	2001-1582E	Full Sized Scattering Bar Alt-PSM Technique for IC Manufacturing in Sub-Resolution ERA	2/19/04	Recorded 013148/0435 at the parent application USP6,711,732
18	10/680,577	2001-1701B	SRAM Cell Design for Soft Error Rate Immunity	10/7/03	Recorded 013408/0285 at the parent application USP6,649,456
19	10/682,269	2002-0026B	Asymmetrical Reset Transistor with Double-Diffused Source for CMOS Image Sensor	10/9/03	Recorded 013422/0370 at the parent application USP6,642,076

Date: December 27, 2004
Chien-Wei (Chris) Chou
Director - Intellectual Property Division